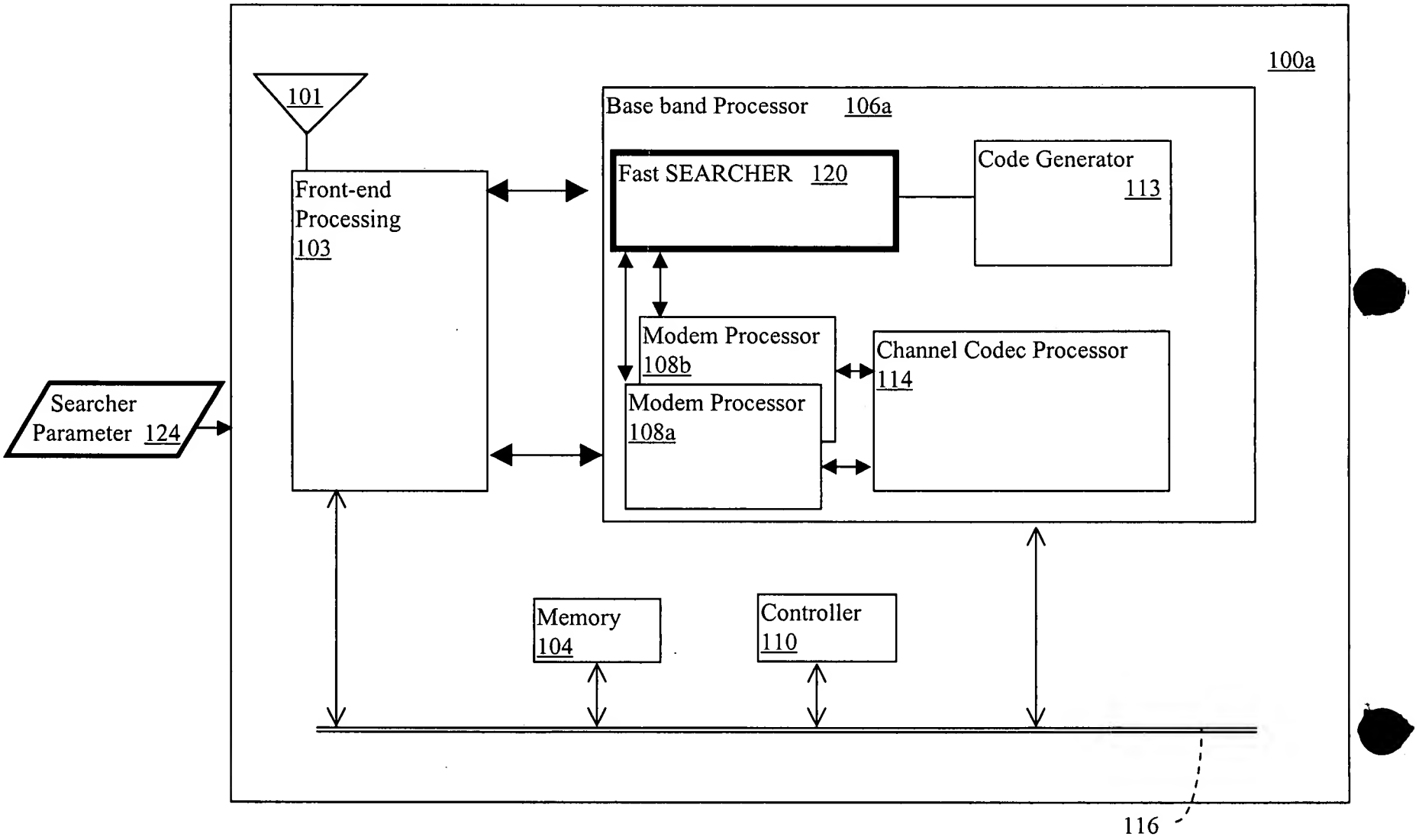
100a
101
Base band Processor 106a
Front-end Processing 103
Fast SEARCHER 120
Code Generator 113
Modem Processor 108b
Channel Codec Processor 114
Modem Processor 108a
Searcher Parameter 124
Memory 104
Controller 110
116

**FIGURE 1**

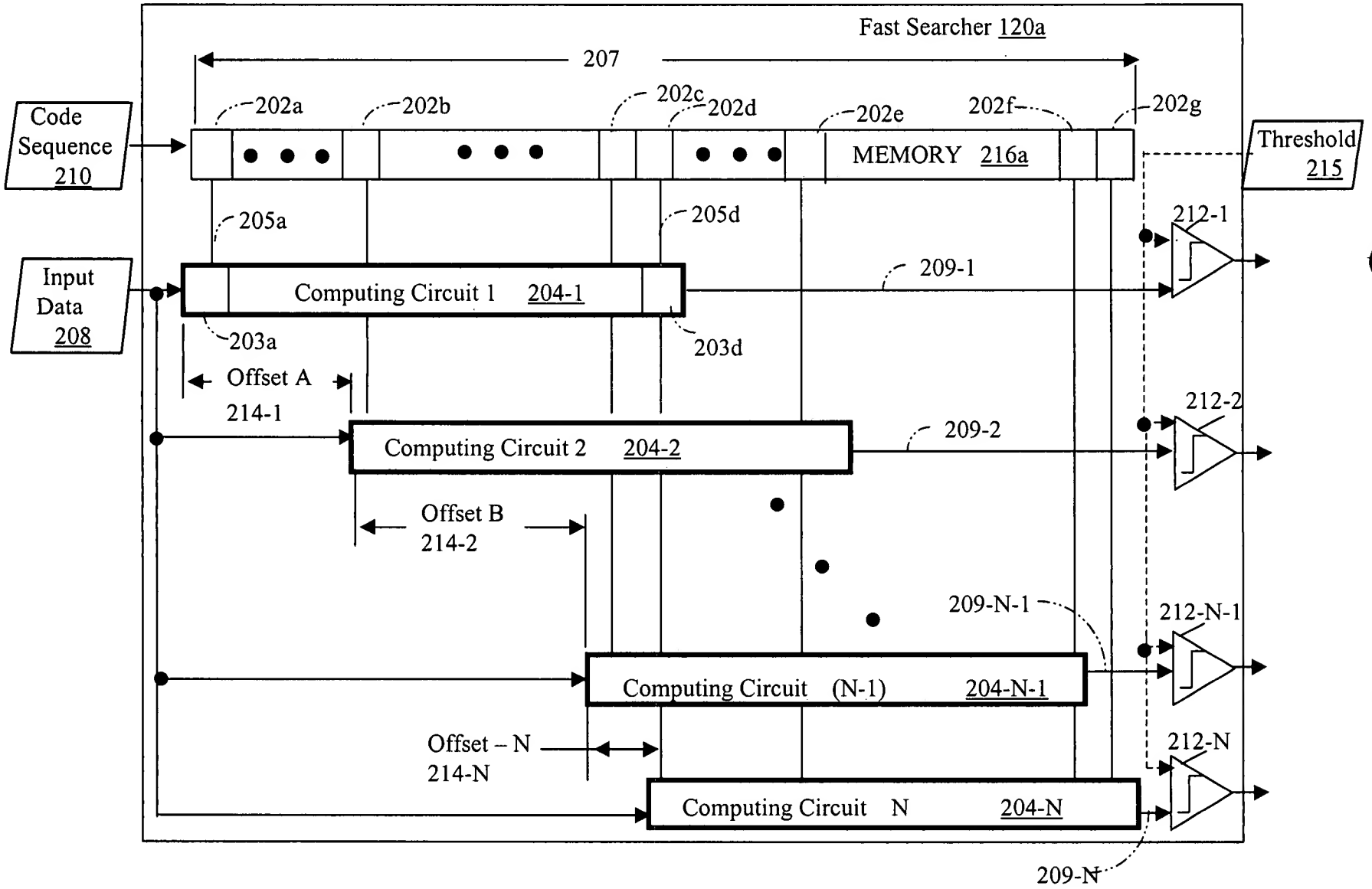
Fast Searcher 120a
207
Code Sequence 210
202a
202b
202c
202d
202e
202f
202g
MEMORY 216a
Threshold 215
205a
205d
212-1
Input Data 208
Computing Circuit 1 204-1
209-1
203a
203d
Offset A 214-1
212-2
Computing Circuit 2 204-2
209-2
Offset B 214-2
209-N-1
212-N-1
Computing Circuit (N-1) 204-N-1
Offset – N 214-N
212-N
Computing Circuit N 204-N
209-N

**FIGURE 2A**

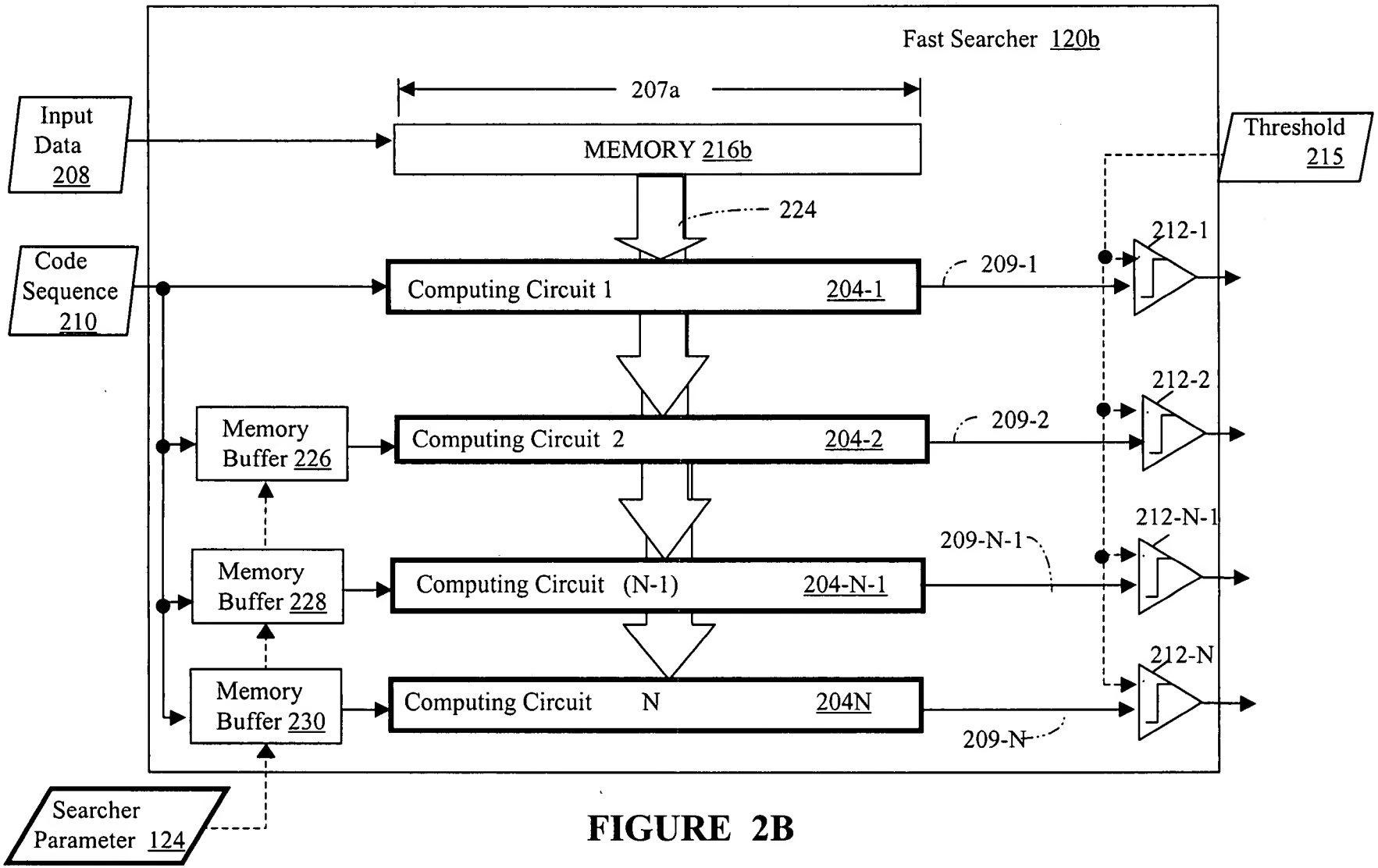
Fast Searcher 120b
207a
Input Data 208
MEMORY 216b
Threshold 215
224
Code Sequence 210
Computing Circuit 1 204-1
209-1
212-1
Memory Buffer 226
Computing Circuit 2 204-2
209-2
212-2
Memory Buffer 228
Computing Circuit (N-1) 204-N-1
209-N-1
212-N-1
Memory Buffer 230
Computing Circuit N 204N
209-N
212-N
Searcher Parameter 124

**FIGURE 2B**

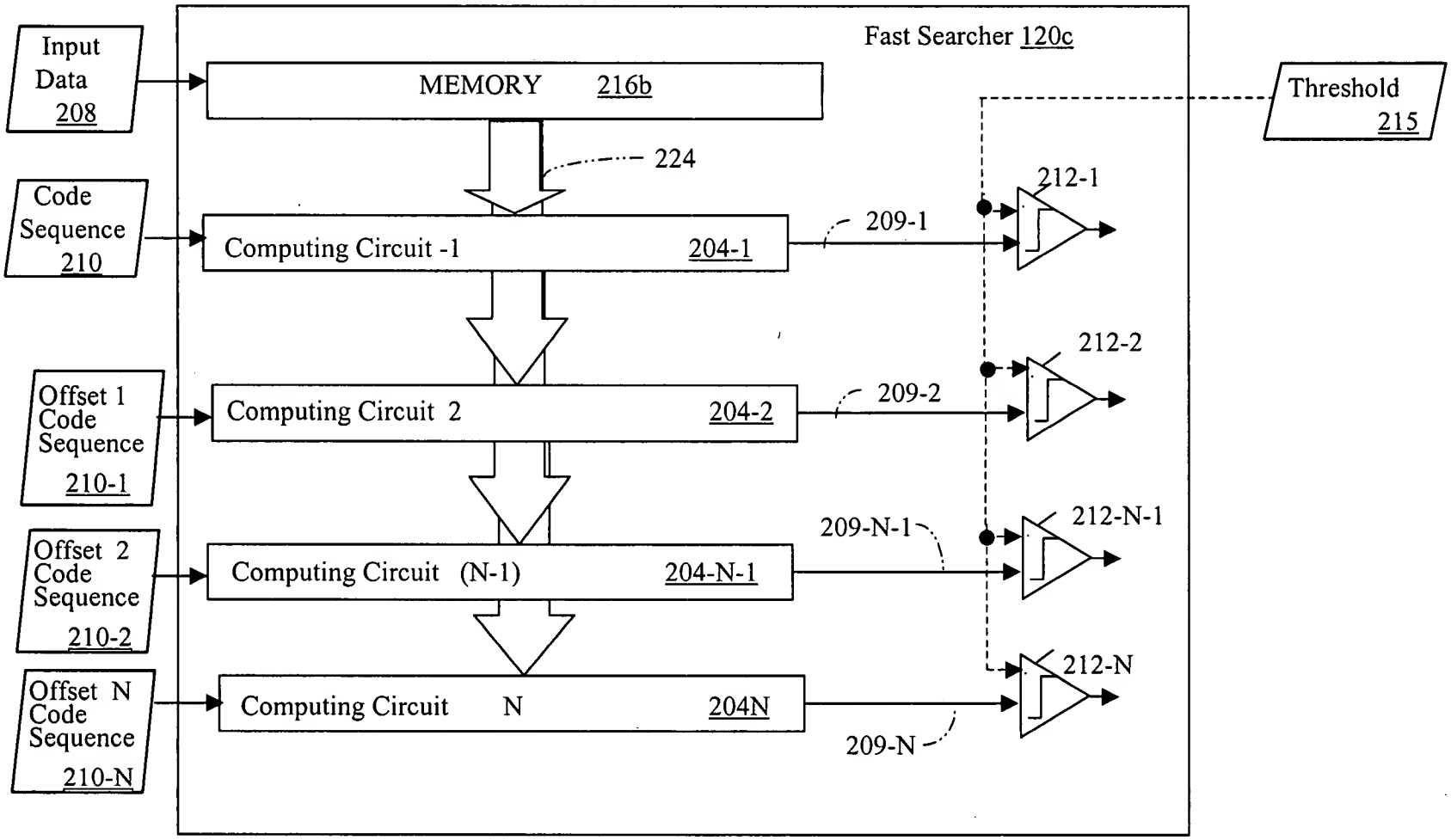
Fast Searcher 120c
Input Data 208
MEMORY 216b
Threshold 215
224
Code Sequence 210
Computing Circuit -1 204-1
209-1
212-1
Offset 1 Code Sequence 210-1
Computing Circuit 2 204-2
209-2
212-2
Offset 2 Code Sequence 210-2
Computing Circuit (N-1) 204-N-1
209-N-1
212-N-1
Offset N Code Sequence 210-N
Computing Circuit N 204N
209-N
212-N

**FIGURE 2C**

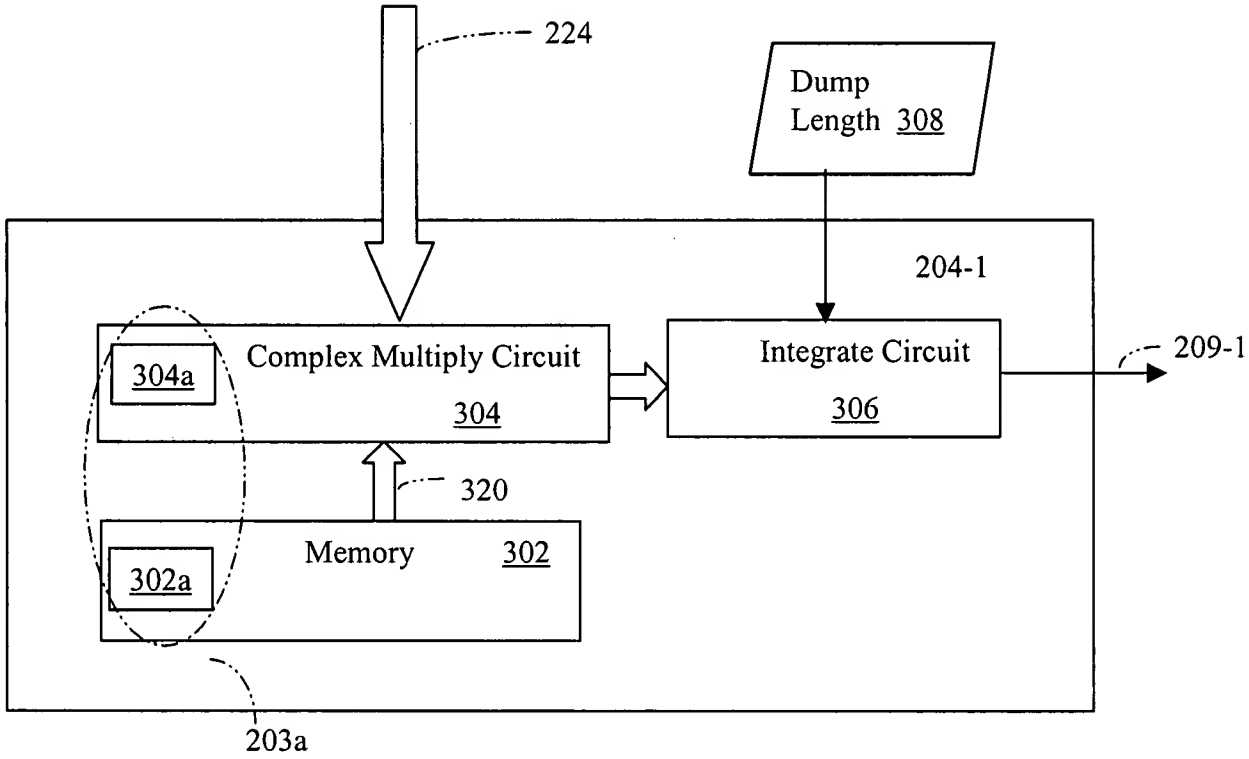
224
Dump
Length 308
204-1
304a
Complex Multiply Circuit
304
Integrate Circuit
306
209-1
320
Memory
302
302a
203a

**FIGURE 3**

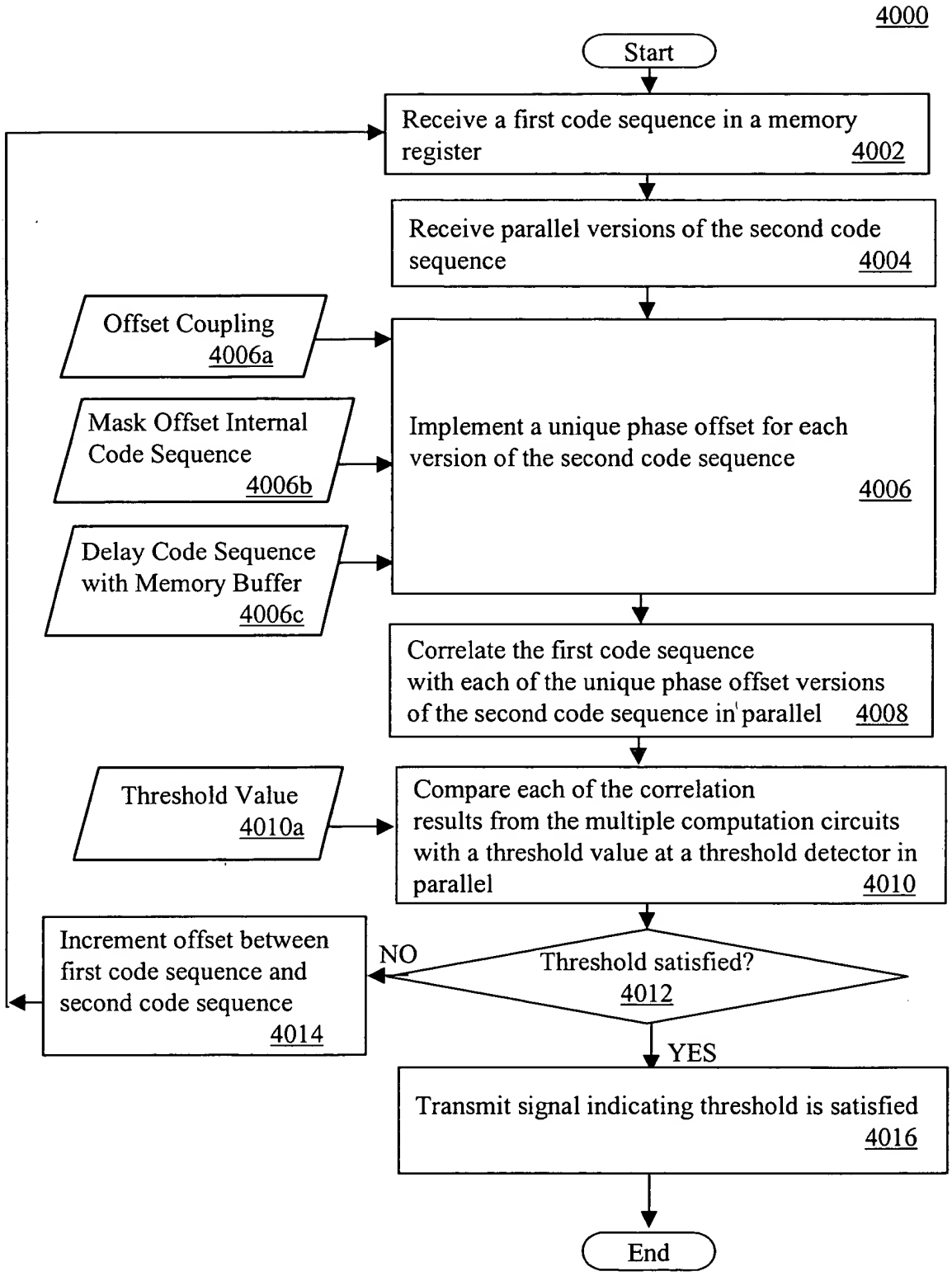
4000
Start
Receive a first code sequence in a memory register 4002
Receive parallel versions of the second code sequence 4004
Offset Coupling 4006a
Mask Offset Internal Code Sequence 4006b
Delay Code Sequence with Memory Buffer 4006c
Implement a unique phase offset for each version of the second code sequence 4006
Correlate the first code sequence with each of the unique phase offset versions of the second code sequence in parallel 4008
Threshold Value 4010a
Compare each of the correlation results from the multiple computation circuits with a threshold value at a threshold detector in parallel 4010
Threshold satisfied? 4012
NO
YES
Increment offset between first code sequence and second code sequence 4014
Transmit signal indicating threshold is satisfied 4016
End

FIGURE 4A